REMARKS

In accordance with the foregoing, the abstract has been amended so that it does not recite any benefits of the applicants' invention, in compliance with MPEP 608.01(b). No new matter is presented in this Amendment.

REJECTIONS UNDER 35 U.S.C. §103:

Claims 1-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over <u>Inoue</u> (U.S. Patent No. 5,696,774) in view of <u>Arai</u> (U.S. Pat. No. 5,757,824). Claim 1 of the instant application claims the following:

"An apparatus generating an error flag, the apparatus comprising:

(1)   a frame-sync error memory which stores frame-sync error information for at least one data block;

(2)   a BIS (Burst Indicator Subcode) error flag memory which stores a BIS error flag for the at least one data block; and

(3)   an error flag generator, which generates an error flag indicating an error existence/absence for ECC (Error-Correction Coding) data with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory."

In the office action at page 2, the Examiner states that <u>Inoue</u> teaches the first two elements of claim 1, and that <u>Arai</u> teaches the third element of claim 1. Then the Examiner supplies the following rationale to reject claim 1 of the instant application:

"Therefore, it would have been obvious to a person of ordinary skill in the art, at the time of the invention to incorporate the error flag generator (57) as taught by <u>Arai</u> in the digital signal recording device, as disclosed by <u>Inoue</u>. Doing so would provide a configuration of an error correction code and a decoding apparatus, which is highly capable of error correction without great quality deterioration of a reproduction signal even when there are many code errors (col. 2, lines 16-20) [in <u>Arai</u>]."

As a general matter, in order to establish a *prima facie* obviousness rejection, the Examiner needs to provide both the existence of individual elements corresponding to the recited limitations, and a motivation to combine the individual elements in order to create the

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recited invention. MPEP 2143. Should the Examiner fail to provide evidence that all of the individual elements or the motivation to combine these elements does not exist in the prior art, then the Examiner has not provided sufficient evidence to maintain a *prima facie* obviousness rejection of the claim. MPEP 2143.03. Thus, the burden is initially on the Examiner to provide evidence as to why one of ordinary skill in the art would have been motivated to combine the individual elements to create the recited invention, and to demonstrate that this evidence existed in the prior art. MPEP 2143.01.

The Examiner Has Not Demonstrated That Each Element Exists In the Prior Art

It is respectfully submitted that the Examiner has not demonstrated that all the claim limitations are taught or suggested by the two cited prior art references Inoue and Arai. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. MPEP 2143.03. In this case, the Examiner has failed to show that at least elements (1) and (3) of the instant application are present in the prior art. Specifically, the Examiner has at least failed to show that Inoue discloses element (1) of the instant application, a frame-sync error memory which stores frame-sync error information for at least one data block, and the Examiner has also at least failed to show that Arai discloses element (3) of the instant application, a code error correction apparatus including an error flag generator (57) which generates an error flag indicating an error existence/absence for ECC (Error-Correction Coding) data with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory.

Element 1

The Examiner has not demonstrated that the prior art contains element (1) as claimed in the instant application. Element (1) of claim 1 in the instant application is a "frame-sync error memory which stores frame-sync error information for at least one data block." The Examiner has argued that Inoue discloses a frame-sync error memory which stores frame-sync error information for at least one data block in col. 51, line 55 through col. 53, line 3. However, the only two references to a "data block" throughout col. 51, line 55 through col. 53, line 3, in Inoue arise in the following passage:

> "The two-track data block of 245 sync blocks configured at the second data synthesizer 119 is stored in a predefined address in the tenth memory 122. The 18x speed playback data and the C5 check code appended to the special playback data for the respective playback speeds having been stored in the memory in the second data synthesizer 119

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are also read from the second data synthesizer 119 at the same timing as the two-track data block, and stored in predefined addresses in the tenth memory 122."

This "two-track data block of 245 sync blocks" in Inoue is generated from transport packets, and these transport packets are used to store information "concerning" a digital video signal, a digital audio signal, and digital data (Inoue, col. 17, lines 50-56). Inoue does not disclose that the information "concerning" a digital video signal, digital audio signal, and digital data concerns frame-sync error information, as claimed in claim 1 of the instant application. Instead, Inoue discloses that the information "concerning" a digital video signal, digital audio signal, and digital data is identification data concerned with identifying whether data in the transport packet is one of these types of data (Inoue, col. 17, lines 60-67). Information which identifies data is not the same as information regarding errors. Therefore, it is respectfully submitted that the Examiner has not demonstrated that the prior art references disclose element (1) of claim 1 in the instant application.

Element 3

The Examiner has also not demonstrated that the prior art contains element (3) of claim 1 in the instant application. Element 3 of claim 1 in the instant application is "an error flag generator, which generates an error flag indicating an existence/absence for ECC (Error-Correction Coding) data with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory." By way of review, FIG. 17 of Arai illustrates an example of a configuration of a flag processing circuit 48 found in a tenth embodiment of Arai. Reference numeral 57 represents an error flag or "high" level generator (col. 12, lines 62-65). The error flag generator 57 is connected to a selector 54, the selector 54 is connected to a control circuit 58, the control circuit 58 is connected to a NAND gate 60, and the NAND gate 60 is connected to an inverter 59 (FIG. 17; col. 12, lines 62-65). When the signal from the NAND gate 60 is "low," the control circuit 58 switches the data selector 54 to the error flag generator 57, and to the error flag (second error flag) derived from the inner code decoding circuit 34 otherwise. As a result, when the first error flag read out of an error flag memory 38 is "low," a high signal is produced from the error flag generator 57 (col. 12, lines 66-67 to col. 13, lines 1-6). The error flag memory 38 stores an error flag attached to the inner code block by the inner code decoding circuit (col. 9, lines 8-10).

There is no mention anywhere in Arai that the error flag generator 57 generates an error

flag indicating an existence/absence for ECC (Error-Correction Coding) data <u>with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory</u>, as claimed in claim 1 of the instant application. The error flag generator in the instant application generates an error flag for erasure correction using the frame-sync error information stored in the frame-sync error memory 130 and the BIS error flag stored in the BIS error flag memory 160 (operation 260). Paragraphs [0026], [0039]. The error flag generator 57 in <u>Arai</u>, on the other hand, uses read outs from the error flag memory 38. Col. 13, lines 3-6. These readouts from the error flag memory 38 in <u>Arai</u> are not readouts "with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory." Instead, the readouts in <u>Arai</u> are based on errors detected in a first and second decoding of inner code blocks. <u>Arai</u>, col. 12, lines 4-27. The inner code blocks in <u>Arai</u> which the error flag generator 57 in <u>Arai</u> uses to generate error flags are not BIS error flags stored in the BIS error flag memory, as recited in claim 1 of the instant application. In other words, the error flag generator of claim 1 in the instant application generates error flags based on a different type of data than the error flag generator 57 disclosed in <u>Arai</u>. Thus, it is respectfully submitted that the Examiner has not demonstrated that the prior art contains each element of claim 1 in the instant application, and therefore the Examiner has not established a *prima facie* case of obviousness. MPEP 2143.03.

The Examiner Has Not Demonstrated a Motivation to Combine <u>Inoue</u> with <u>Arai</u>

Assuming *arguendo* that the Examiner has shown that all the individual elements of the recited limitations are present in the prior art, it is respectfully submitted that the Examiner has failed to provide a motivation to combine the individual elements from the prior art to arrive at applicants' claimed invention. In order to establish a *prima facie* case for obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. MPEP 2143. There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. MPEP 2143.01. The initial burden is on the Examiner to provide some suggestion of the desirability of doing what the inventor has done. MPEP 2142.

As mentioned earlier, the Examiner has argued that:

"...it would have been obvious to a person of ordinary skill in the art, at the time of the invention to incorporate the error flag generator (57) as taught by Arai in the digital signal recording device, as disclosed by Inoue. Doing so would provide a configuration of an error correction code and a decoding apparatus, which is highly capable of error correction without great quality deterioration of a reproduction signal even when there are many code errors (col. 2, lines 16-20) [in Arai]."

It is respectfully submitted that the Examiner has failed to carry his burden in establishing a *prima facie* case of obviousness, because the Examiner has failed to show the desirability of incorporating the error flag generator 57 of Arai with the digital signal recording device of Inoue.

The error flag generator 57 in Arai is part of a second configuration of the flag processing circuit 48, which is a component in the tenth embodiment of Arai. Col. 12, lines 62-65. The purpose of the tenth embodiment in Arai is to provide an embodiment which requires only one check information address for each inner code block, regardless of the number of times of reproduction of the product code block. Col. 11, lines 58-65. By providing an embodiment which requires only one check information address for each inner code block, regardless of the number of times of reproduction of the product code block, Arai discloses a code error correction apparatus with a high correction ability and a low memory capacity. Col. 13, lines 7-12.

Inoue, on the other hand, discloses a digital signal playback device with improved error correction capability in both normal playback speed and fast playback speed. Col. 5, lines 44-52. Inoue is not directed towards an invention with a decreased memory capacity. Although the Examiner is correct in asserting that one purpose of Arai is to provide a "configuration of an error correction code and decoding apparatus which is highly capable of error correction without great quality deterioration of a reproduction signal even when there are many code errors," Arai, col. 2, lines 16-20, another purpose of Arai is to provide such a configuration using a low memory capacity. As mentioned above, Arai achieves this second purpose, a low memory capacity, in a tenth embodiment by using an error flag generator 57 as a component in a flag processing circuit 48. Col. 12, lines 62-65. Arai clearly states that the purpose for this tenth embodiment is to provide an embodiment which has "a high correction ability...by use of a memory having a capacity equivalent to approximately one product code block," in other words, by use of a memory having a low memory capacity. Col. 13, lines 7-10.

One skilled in the art would not be motivated to combine an invention designed to have a low memory capacity (Arai) with an invention designed to improve error of both fast and normal

playback speed of a digital signal playback device (Inoue), without an explicit reason for doing so. The two inventions disclosed in Inoue and Arai are directed at solving different problems. Inoue is directed at improving the quality of both normal and fast playbacks speeds. Arai is directed at providing a code error correction apparatus which reduces code error using a low memory capacity. One skilled in the art would have no reason to combine the digital signal playback device of Inoue with the lower memory capacity of Arai, because decreasing memory capacity has nothing to do with improving playback quality at both normal and fast speeds.

Moreover, there is nothing in Arai that suggests that the error flag generator 57 itself contributes to a configuration of an error correction code and a decoding apparatus, which is highly capable of error correction without great quality deterioration of a reproduction signal even when there are many code errors. Arai, col. 2, lines 16-20. Rather, the error flag generator is simply one of many components used in one configuration of the flag processing circuit 48. The mere existence of an error flag generator 57 in Arai, without more, does not provide a motivation or suggestion to one skilled in the art to specifically combine the error flag generator 57 in Arai with the digital signal recording device of Inoue. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art suggests the desirability of that combination. MPEP 2143.01 (III). Here, the mere fact that the error flag generator 57 of Arai might possibly be combined with the digital signal recording device of Inoue does not render the resultant combination obvious. If otherwise, Examiners could reject virtually any claims simply because prior art references can be combined to arrive at virtually any resultant combination. The mere fact that such resultant combinations can be achieved is not a valid ground for rejecting a claim under 35 U.S.C. §103. MPEP 2143.01 (III).

Although Arai does suggest that the tenth embodiment generally secures a "high correction ability...by use of a memory having a capacity equivalent to approximately one product code block, while at the same time permitting re-detection of a false detection or correction, thereby improving the reliability of the reproduction of digital information," Col. 13, lines 7-12, this general assertion of an alleged advantage of an entire embodiment does not equate to a suggestion or motivation to combine one small component of the tenth embodiment with another reference. Considering the multitude of different components used in the tenth embodiment of Arai, the Examiner has provided insufficient evidence of a motivation to combine the error flag generator 57 of Arai with the digital signal recording device of Inoue.

Based on the foregoing, this rejection is respectfully requested to be withdrawn.

Additionally, since the Examiner relied on the above-mentioned rationale to reject the remaining claims 2-18 in the instant application, it is respectfully requested that the remaining rejections of claims 2-18 be withdrawn as well.

CONCLUSION:

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

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